TangerineSDR Clock Module Status Report

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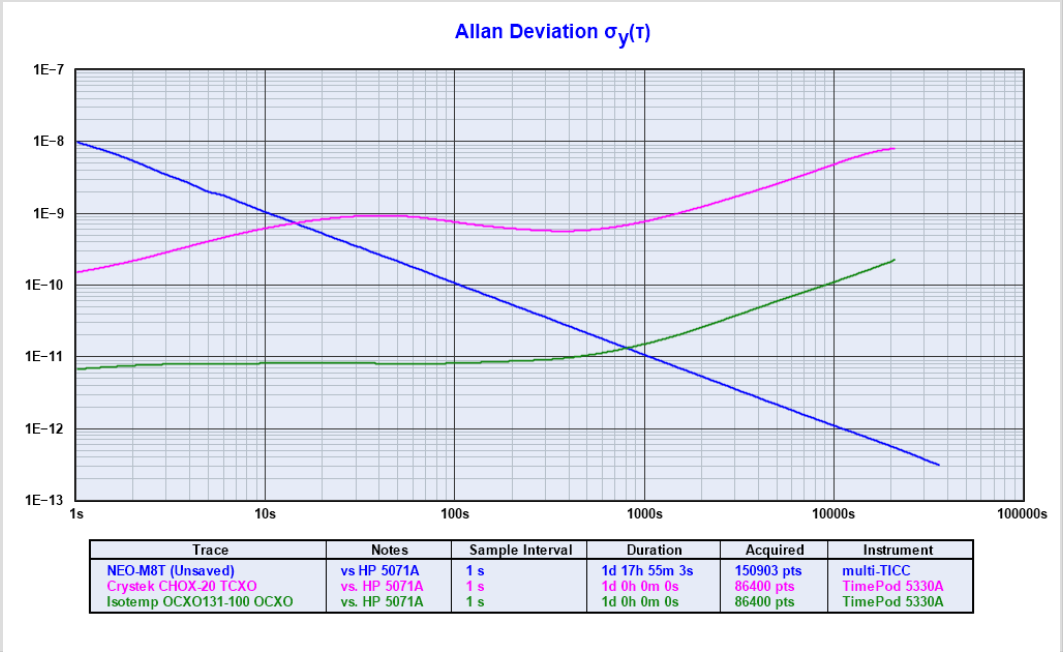
Clock Module Overview

- GPS Disciplined Oscillator providing an *accurate* and *stable* source of:
  - 122.88 MHz for receiver ADC and transmitter DAC
  - 1 PPS for timestamping
  - TOD message
  - Multiple synthesized outputs from 100 Hz to 1024 MHz
- **Usable separately from TangerineSDR** via interface board for the time-nuts (tentative name: SynthDO)

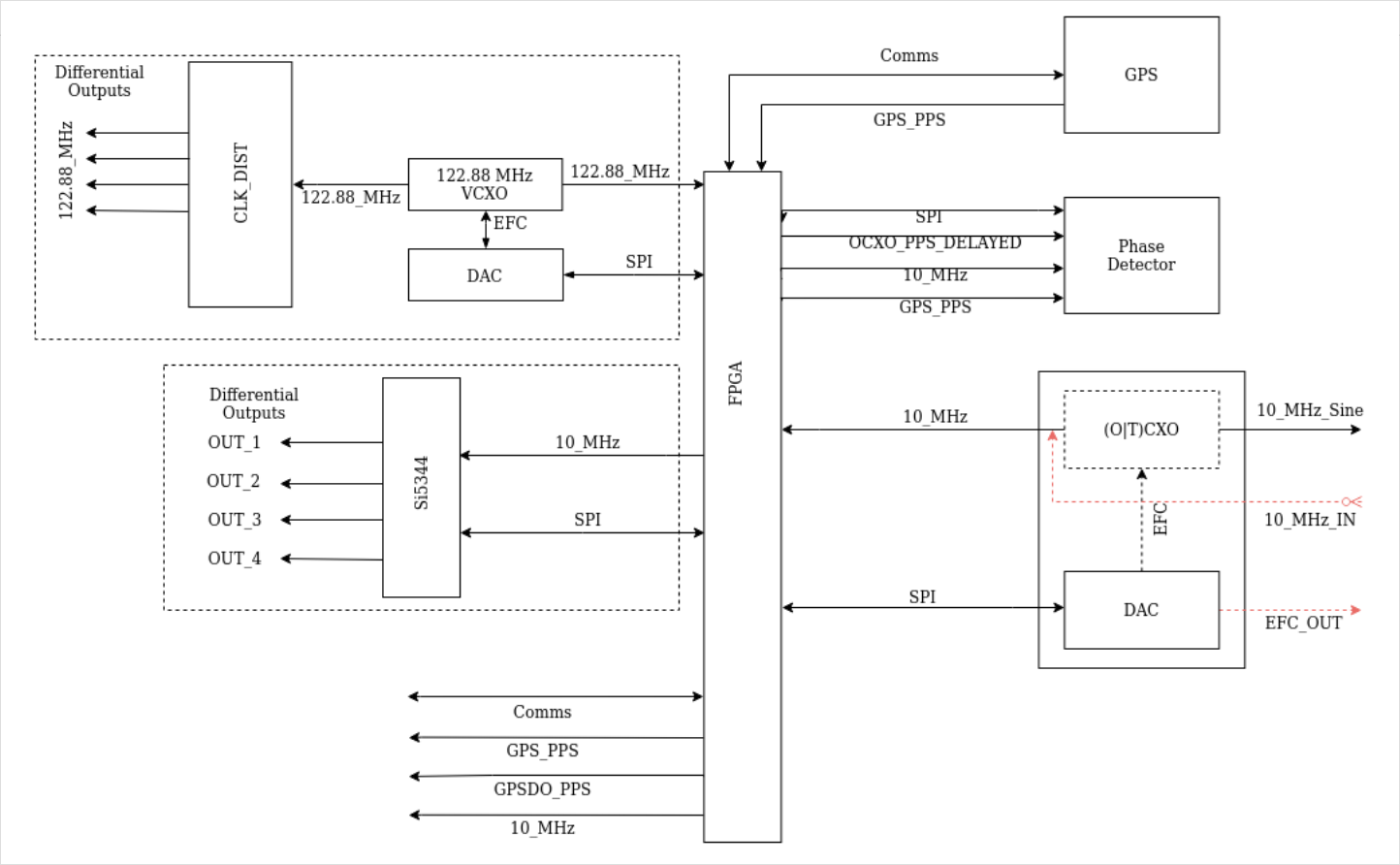
Refresher: What's a GPSDO?

- GPS noisy at short term but tracks USNO/NIST in the long run
- XO stable in the short term, but drifts
- Best of both worlds: use PLL to steer XO with GPS
- Loop bandwidth tuned to ADEV "crossover" point



Trace	Notes	Sample Interval	Duration	Acquired	Instrument
NEO-M8T (Unsaved)	vs HP 5071A	1 s	1d 17h 55m 3s	150903 pts	multi-TICC
Crystek CHOX-20 TCXO	vs. HP 5071A	1 s	1d 0h 0m 0s	86400 pts	TimePod 5330A
Isotemp OCXO131-100 OCXO	vs. HP 5071A	1 s	1d 0h 0m 0s	86400 pts	TimePod 5330A

Clock Module Hardware Block Diagram – Mark I



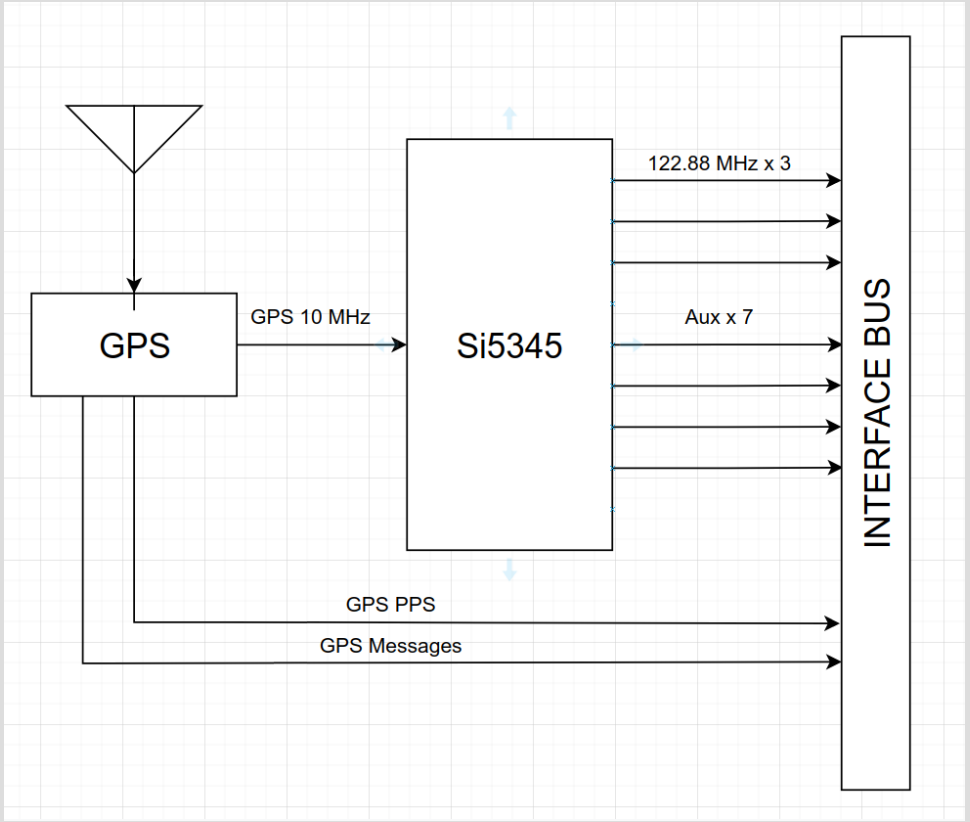
Redesign!

- Extensive tests on modern GPS receivers revealed a simpler way
- Ublox “TIMEPULSE” need not be PPS; can be >10 MHz
  - ADEV is remarkably good (better than PPS)
  - Phase noise sucks
- “Jitter Attenuator” chips (e.g., SiLabs 5345) are neat:
  - Can clean up PN of dirty input
  - Include narrow bandwidth PLL
  - External oscillator sets short term and holdover performance
  - Multiple outputs at 100 kHz to 1028 MHz

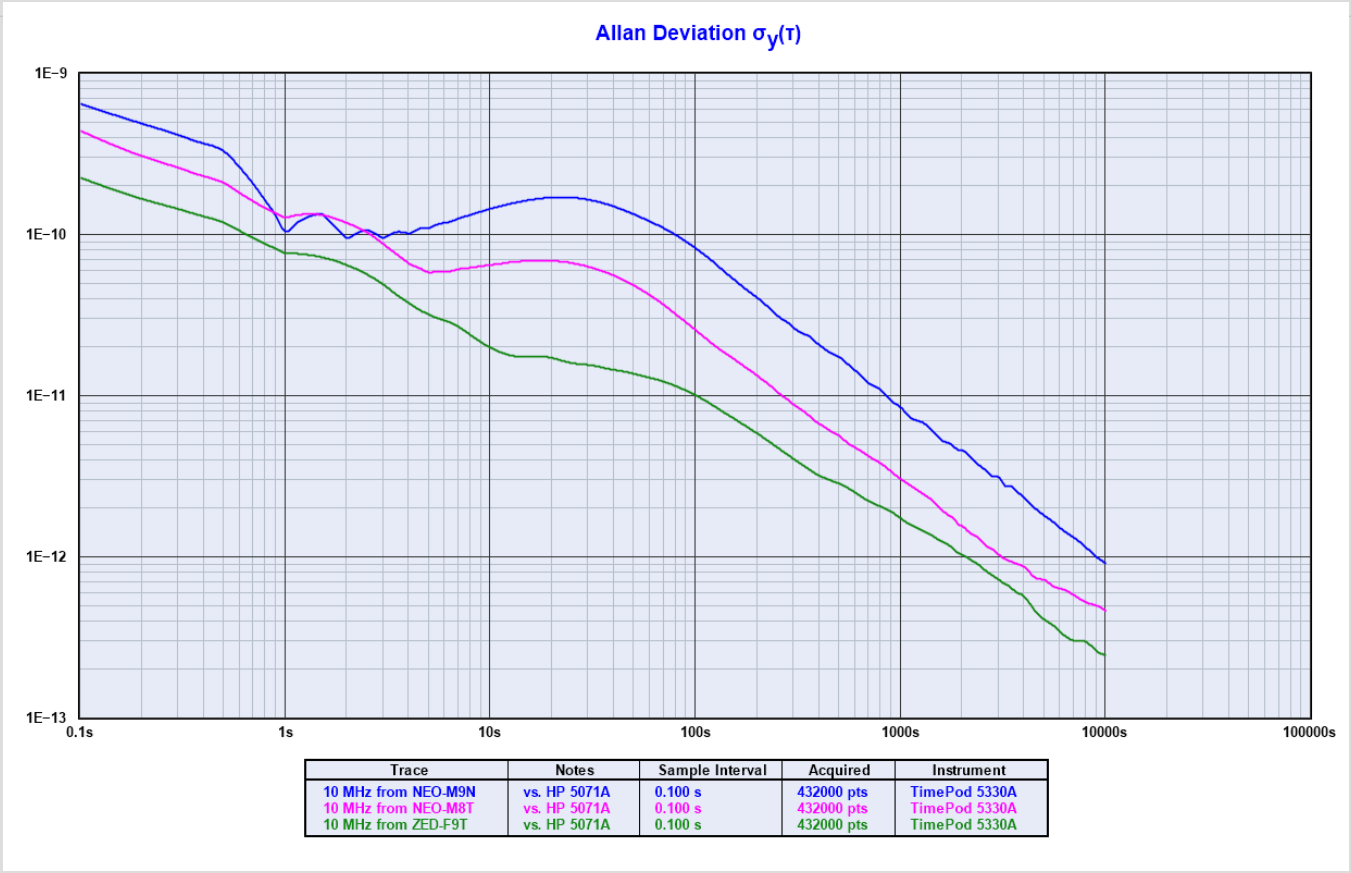
Enter CKM Mk II

- uBlox GPS 10 MHz TIMEPULSE is input signal to Si5345
  - ‘5345 PLL acts like the back half of a GPSDO
  - Output is locked to nominal 10 MHz input
    - Actually, input can be any freq the GPS module can generate, so if needed we can move to avoid interference
    - Phase noise is cleaned up
- Si5345 has 10 (!) independent outputs and can directly provide all TangerineSDR clocks plus other uses

Clock Module Hardware Block Diagram – Mark II

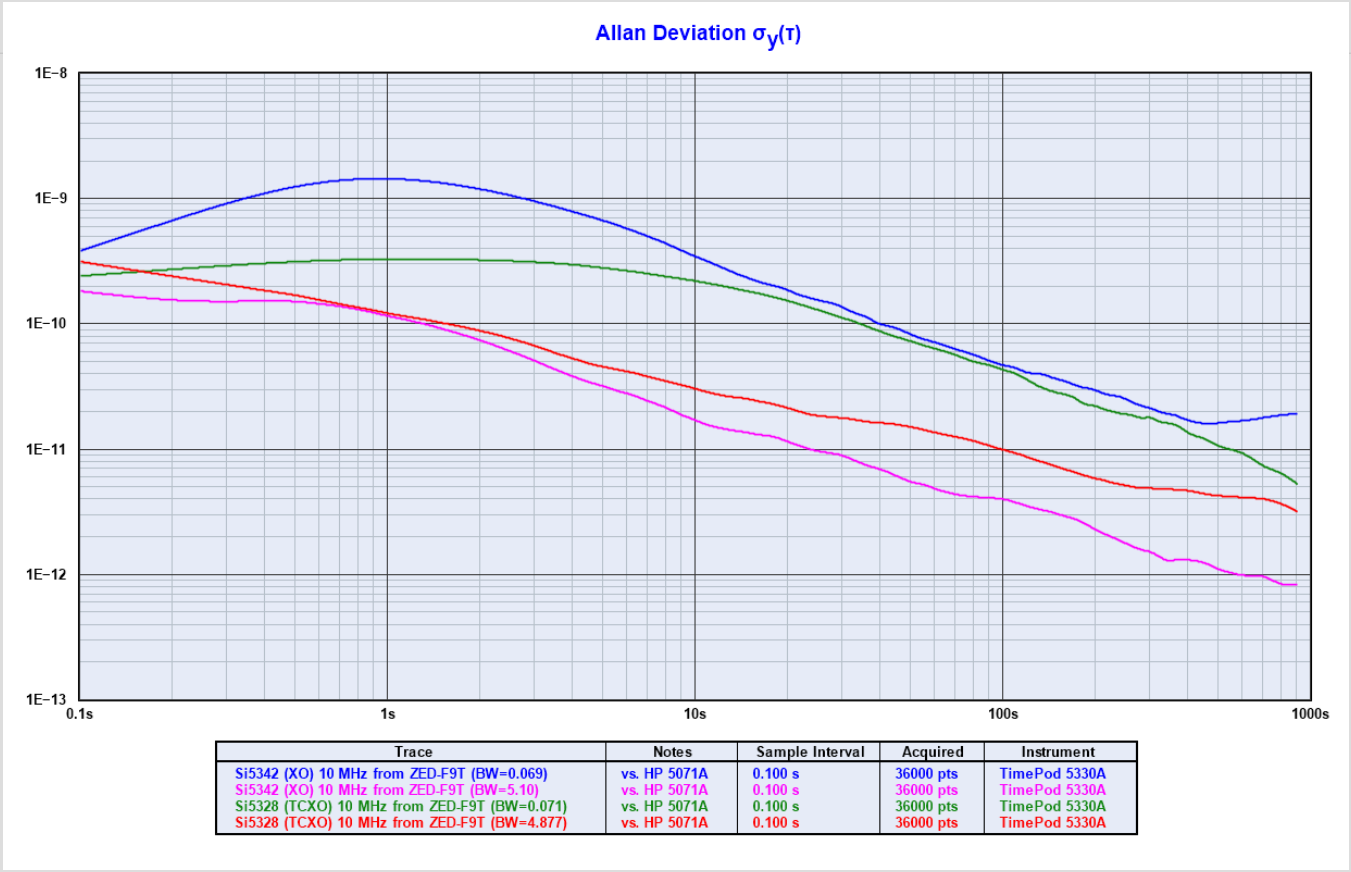


uBlox GPS Receiver
10 MHz Performance



Trace	Notes	Sample Interval	Acquired	Instrument
10 MHz from NEO-M9N	vs. HP 5071A	0.100 s	432000 pts	TimePod 5330A
10 MHz from NEO-M8T	vs. HP 5071A	0.100 s	432000 pts	TimePod 5330A
10 MHz from ZED-F9T	vs. HP 5071A	0.100 s	432000 pts	TimePod 5330A

Ublox 10 MHz SiLabs Evaluation Boards



Trace	Notes	Sample Interval	Acquired	Instrument
Si5342 (XO) 10 MHz from ZED-F9T (BW=0.069)	vs. HP 5071A	0.100 s	36000 pts	TimePod 5330A
Si5342 (XO) 10 MHz from ZED-F9T (BW=5.10)	vs. HP 5071A	0.100 s	36000 pts	TimePod 5330A
Si5328 (TCXO) 10 MHz from ZED-F9T (BW=0.071)	vs. HP 5071A	0.100 s	36000 pts	TimePod 5330A
Si5328 (TCXO) 10 MHz from ZED-F9T (BW=4.877)	vs. HP 5071A	0.100 s	36000 pts	TimePod 5330A

Tradeoffs

- Pros:
  - Much simpler design
  - No FPGA programming required
  - Lower cost makes using better GPS less painful
  - Huge frequency agility
- Cons:
  - XO frequency used limits oscillator choices
  - Loop bandwidth won’t optimize very high quality XOs
  - PPS holdover/sync more complicated

More About Holdover

- Output accuracy when GPS lock is lost
  - Usually specified by XX XS of time error after XX hours
  - Primarily a timing concern (big deal for telcos)
- Traditional GPSDO generates PPS from the XO to drive phase detector
  - XO_PPS is sync'd to GPS_PPS via PLL
  - XO_PPS is the unit output PPS
    - Has less jitter than GPS_PPS
  - If lock is lost, PPS output continues
    - Smoothly and without phase change, subject to XO drift
    - That's holdover mode

More About Holdover

- CKM Mark II doesn’t generate XO-based PPS
- ZED-F9T and NEO-M8T have two TIMEPULSE outputs
  - One set to nominallly 10 MHz to drive synth chip
  - Other TIMEPULSE provides PPS
    - ZED-F9T: +/- 4 ns jitter; NEO-M8T: +/- 11 ns
  - NEO-M9N has only one TIMEPULSE used for RF, so no PPS
- We configure TIMEPULSE outputs to stop on LoL
  - Si5345 goes into holdover; outputs remain locked to TCXO
  - But what about PPS?

More About Holdover

- Implement a counter to generate “XO_PPS” from one of the synthesizer RF outputs
  - Where? On CKM module? On Data Engine?
- Sync of XO_PPS to GPS_PPS will result in a minimum of one counter clock cycle delay
  - 10 MHz = 100 ns, 100 MHz = 10 ns, etc.
  - How high a clock is practical?
- Need to resync after holdover
  - How quickly do we slew XO_PPS to match GPS_PPS?
    - This isn’t an issue at startup, when we can jam-sync
    - Need user input on how best to handle

March 2021 Status

- Proof-of-Concept requires finishing some test fixtures
  - Testing with 5328 and 534x evaluation boards gives high confidence of ultimate performance, but need to mate TCXO with 534x to see everything working together
- John’s schematic completed and turned over to Scotty to put into production CAD tools
- Board layout will begin shortly
- “time-nuts” carrier board not started yet